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PRESS RELEASE

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A 'smart' chip that reduces both consumption and computing time marks a breakthrough in high-performance computing at Politecnico di Milano

The study by the researchers of the Department of Electronics, Information and Bioengineering – DEIB published in *Nature Electronics*

Milan, 20 January 2026 - Dramatically reducing energy consumption while accelerating the processing of large amounts of data. This is the aim of the new chip developed by a group of researchers from the **Department of Electronics, Information and Bioengineering – DEIB** at the Politecnico di Milano, led by Professor **Daniele Ielmini**, and presented in the study published in the prestigious journal ***Nature Electronics***, with the researcher **Piergiulio Mannocci** as the first author.

The work originated as part of the **ANIMATE** *(ANalogue In-Memory computing with Advanced device TEchnology*) project, which was awarded an **ERC Advanced Grant** in 2022 and drew on Daniele Ielmini's preliminary research into **CL-IMC** (*Closed-Loop In-Memory Computing*) and the opportunities it could offer, i.e. faster solving of calculations and use of up to **5,000 times less energy than digital computers**. The goal of the ANIMATE project was to develop the technology for the device, the circuits and system architectures, and the set of applications to validate the CL-IMC.

The resulting chip makes use of in-memory computing, which aims to **overcome a limitation of computers: the need to continuously move data between the memory and the processor**. **By eliminating this internal 'traffic', the systems become faster** and more energy efficient. In the recently published study, the DEIB team presented **a fully integrated analogue accelerator for solving linear and non-linear systems of equations** designed with CMOS (*Complementary Metal-Oxide-Semiconductor*) technology, implemented as standard for the production of silicon integrated circuits.

The device uses two 64×64 arrays of programmable resistive memories: an array is a kind of 'ordered grid' made up of identical parts arranged in rows and columns, similar to graph paper, where each intersection between a row and a column represents a memory cell. The cells are based on SRAM (*Static Random-Access* Memory) technology, a type of fast and stable memory which in this case is combined with integrated resistors for programming different levels of resistance. The architecture is complemented by an **innovative model of analogue processing** that utilises components integrated in the chip such as operational amplifiers and analogue-to-digital converters.

The set allows the system to **handle complex calculations directly in the structure of the memory, avoiding the need to move data to an external processor**, thereby **reducing calculation times** to a significant extent. In tests, the chip achieved similar accuracy to conventional digital systems, but with **lower power consumption, less computing latency and a smaller footprint on the silicon**.

Daniele Ielmini, a member of DEIB and head of the research group, explained: "The integrated chip demonstrates **the feasibility on an industrial scale of a revolutionary concept such as analogue computation in memory**. We are already working on putting this innovation into use in real-world applications to reduce the energy costs of computation, especially in the field of artificial intelligence".

Piergiulio Mannocci, a researcher for DEIB and first author, commented: "This work is the result of an international collaboration between academia and industry that has also involved **Peking University**, a diverse team involving professors, researchers, PhD Candidates and students, and demonstrates the potential of analogue in-memory computation for high-performance, energy-efficient applications."

The study represents **an important step towards more compact, faster and sustainable devices**, opening up new perspectives for research and industry. In-memory computing is an ideal solution, in fact, in contexts requiring high performance and high energy efficiency such as artificial intelligence, the processing of large volumes of data, and next-generation wireless communication systems. Applications range **from robotics to data centres and from navigation systems to advanced telecommunications networks, such as 5G and the 6G technologies of the future**.

LINK TO THE FULL PUBLICATION

LINK TO THE PHOTO GALLERY

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